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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Li Fung Chang et al. **Examiner**: Juan A. Torres
Serial No: 10/791,945 **Art Group**: 2631
Filing Date: March 3, 2004 **Docket No**: BP3012
Title: INCREMENTAL REDUNDANCY SUPPORT IN A CELLULAR WIRELESS TERMINAL HAVING IR PROCESSING MODULE

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APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

A Notice of Appeal with a Pre-Appeal Brief was filed on April 19, 2006. A Notice of Panel Decision from Pre-Appeal Brief Review was mailed June 16, 2006 with an indication to proceed to the Board of Patent Appeals and Interferences, creating an Appeal Brief Due date of July 16, 2006. Enclosed herewith is a petition for a one-month extension of time under 37 C.F.R. 1.136 and a credit card payment form in the amount of $620 for the Appeal Brief Fee $500 and the one-month extension petition fee of $120, extending the date for filing this Appeal Brief to August 16, 2006. If any petition fee for an extension of time or any other additional fee is required, the undersigned attorney directs the office to debit such fee from deposit account number 50-2126.

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A. Real Party in Interest

All rights to the above referenced patent application have been assigned to:

Broadcom Corporation
16215 Alton Parkway
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B. Related Appeals and Interferences

There are no known other appeals or interferences that would directly or indirectly affect the Board's decision in the present appeal.

C. Status of the Claims

Claims 1-31 are pending. Claims 1, 3-5, 7, 11, 16, 18-20, 22, 26 and 29 stand rejected under 35 U.S.C. 102(e) as being anticipated by Pukkila (US 20010017904 A1). Claims 1-7, 9-11, 13-22, 24-26 and 28-31 stand rejected under 35 U.S.C. 102(e) as being anticipated by Parolari (US 200400811248 A1). Claims 8, 12, 23, and 27 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Parolari in view of Ramesh (U.S. Patent No. 6,909,758 B2).

Claims 1, 12, 27, 16, and 31 are subject to a provisional type double patent rejection over co-pending applications 10/731,803 and 10/791,945. These rejections are not addressed in this Appeal Brief.

D. Summary of claimed subject matter

The claims of the present application are directed towards an architecture and related methodology for Incremental Redundancy (IR) processing by a radio receiver. Generally, IR processing includes a radio transmitter puncturing a coded data block to create various punctured versions of the coded data block and then incrementally transmitting differing (or same) punctured versions of the coded data block to the radio receiver. Upon receipt of each punctured version of the coded data block (except for the first punctured version), the radio receiver combines the received punctured version of the coded data block with one or more previously received punctured version(s) of the coded data block to create a composite coded data block, which is usually still punctured to some degree. The radio receiver then decodes the composite coded data block. When the decoding is successful (verified by error checking of the decoded data block), IR operations result in the receipt of the data block by the radio receiver even though less than the complete coded data block was transmitted.

Claims 1-15 and 16-31 are directed to methods and systems, respectively, for performing IR processing operations in a wireless receiver. In particular, claim 1 describes the sharing of IR processing functions between a system processor and an IR processing module. After baseband processing of a received analog signal to produce soft decision bits of a data block, the system processor configures a plurality of IR processing module registers. The system processor then initiates operation of the IR processing module. The IR processing module accesses the plurality of IR processing modules and then performs IR processing operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

.E. Grounds of rejection to be reviewed on Appeal

1. The rejection of claims 1, 3-5, 7, 11, 16, 18-20, 22, 26, and 29 as being anticipated under 35 U.S.C. 102(b) by Pukkila (US 20010017904 A1).

2. The rejection of claims 1-7, 9-11, 13-22, 24-26, and 28-31 as being anticipated under 35 U.S.C. 102(e) by Parolari (US 20040081248 A1).

3. The rejection of claims 8, 12, 23, and 27 under 35 U.S.C. 103(a) as being unpatentable over Parolari in view of Ramesh (U.S. Patent No. 6,909,758 B2).

F. Argument:

1. Claims 1, 3-5, 7, 11, 16, 18-20, 22, 26, and 29 are not anticipated under 35 U.S.C. 102(b) by Pukkila (US 20010017904 A1).

Independent claim 1 is directed to a "method for performing Incremental Redundancy (IR) operations in a wireless receiver." This method includes:

(a) receiving an analog signal corresponding to a data block;

(b) sampling the analog signal to produce samples;

(c) equalizing the samples to produce soft decision bits of the data block;

(d) configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers;

(e) initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver; and

(f) accessing, by the IR processing module, the plurality of IR processing module registers; and

(g) performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

FIG. 5B of the present application is reproduced below to illustrate how the operations of claim 1 are accomplished by a wireless receiver of the present invention and to distinguish the elements of claim 1 from the cited prior art.

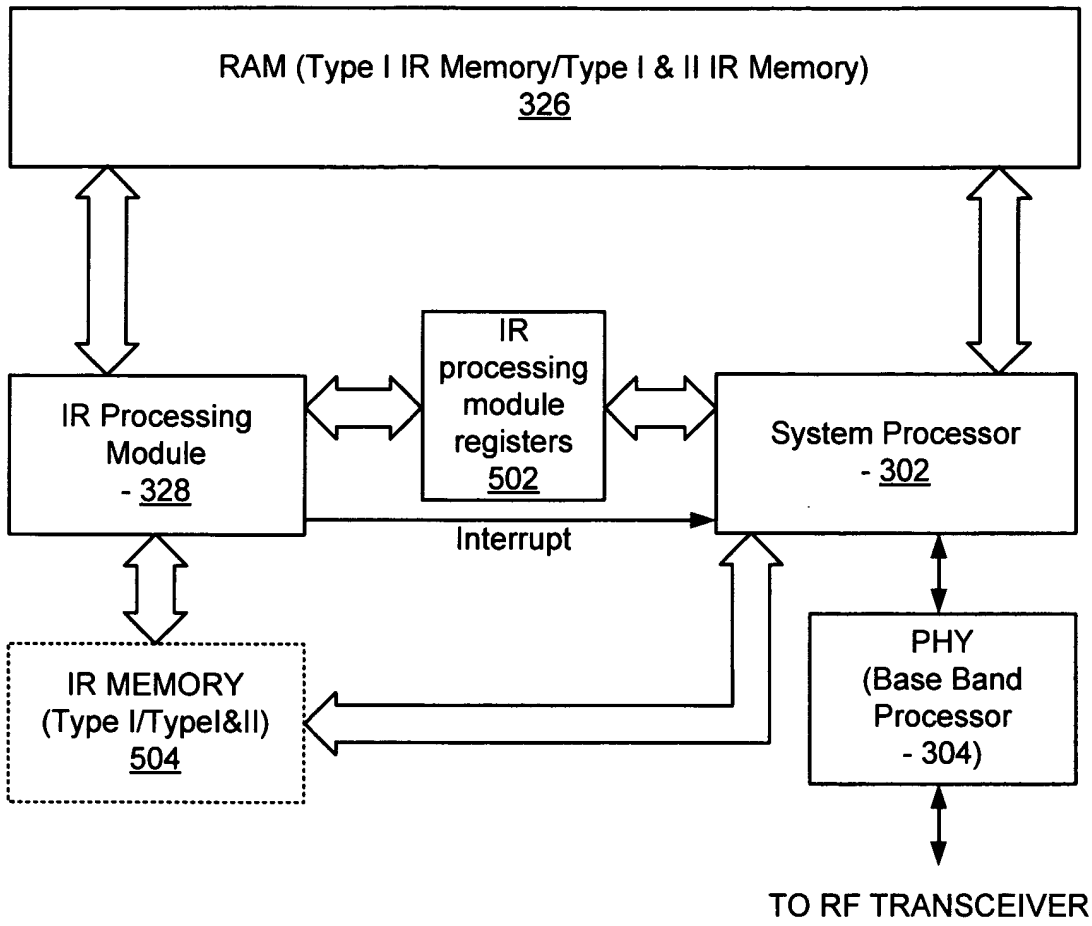

FIG. 5B
(Of the Pending Application Under Appeal)

Relating the blocks of FIG. 5B to the elements of claim 1, the baseband processor 304 performs Physical (PHY) layer operations that include (a) receiving an analog signal corresponding to a data block; (b) sampling the analog signal to produce samples; and (c) equalizing the samples to produce soft decision bits of the data block. The system processor 302 (d) configures the plurality of IR processing module registers 502; and (e) initiates operation of an IR processing module 328 of the wireless receiver. Finally, the IR processing module 328 (f) accesses the plurality of IR processing module registers 502; and (g) performs operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

Generally, Pukkila is directed to iterative equalization and decoding, such that "decoding decisions are fed back as a kind of a priori information into a new signal processing round where the same block of digital data is equalized and decoded anew." Pukkila paragraph [0015]. Thus, Pukkila teaches to iteratively operating on received signals to avoid retransmissions. In contradistinction to the teachings of Pukkila, claim 1 is concerned with how efficiently perform IR processing upon multiple received transmissions.

The Final Office Action cites FIGs. 2 and 3 of Pukkila and related text for its anticipation rejection of claim 1. Shown below is a recreation of FIG. 2 of Pukkila. The Office Action also relies on FIG. 3 of Pukkila, which is not reproduced herein but that illustrates how iterative equalization and decoding operations are performed on received transmissions to avoid retransmissions.

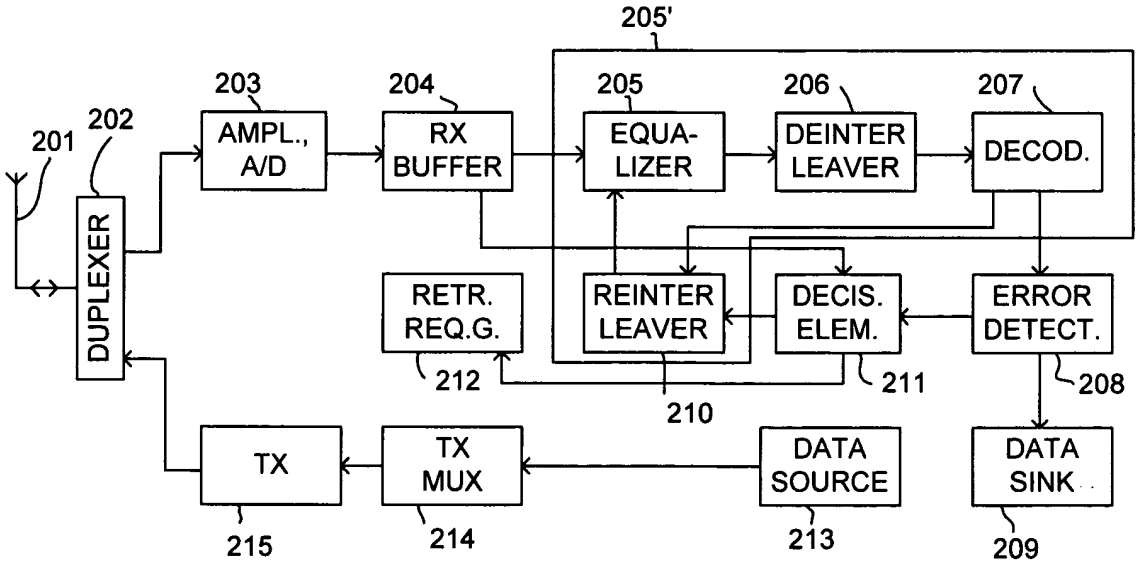

Fig. 2
(of Cited Reference Pukkila)

Applicants concede that Pukkila fairly discloses the elements of (a) receiving, (b) sampling, and (c) equalizing of claim 1. Applicants urge that Pukkila fails to disclose, suggest, or teach the elements of (d) configuring, (e) initiating, (f) accessing, or (g) performing of claim 1.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with (d) "configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers" of claim 1. As Pukkila describes at paragraph [0025], last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Blocks 305-318 of FIG. 3 of Pukkila describe iterative equalization and decoding operations. Block 205' of FIG. 2 of Pukkila and the associated operations of blocks 305-318 of FIG. 3 do not disclose, suggest, or teach (d) "configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers" as required by claim 1.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with (e) "initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver" of claim 1. As previously described, block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations and blocks 305-318 of FIG. 3 of Pukkila describe iterative equalization and decoding operations. These teachings of Pukkila do not disclose, suggest, or teach (e) "initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver" as required by claim 1.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with (f) "accessing, by the IR processing module, the plurality of IR processing

module registers" of claim 1. As previously described, block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations and blocks 305-318 of FIG. 3 of Pukkila describe iterative equalization and decoding operations. These teachings of Pukkila do not disclose, suggest, or teach (f) "accessing, by the IR processing module, the plurality of IR processing module registers" as required by claim 1.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with (g) "performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block." As previously described, block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations and blocks 305-318 of FIG. 3 of Pukkila describe iterative equalization and decoding operations. These teachings of Pukkila do not disclose, suggest, or teach (g) "performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block" of claim 1.

Pukkila fails to anticipate claim 1 for any and all of the reasons provided above. Because claims 3-5, 7, and 11 depend from claim 1, Pukkila fails to anticipate claims 3-5, 7, and 11 for these same reasons. Claims 3-5, 7, and 11 require additional operations by/with the IR processing module and/or the plurality of IR processing module registers. Pukkila fails to disclose the IR processing module and the plurality of processing module registers. Thus, Pukkila fails to anticipate claims 3-5, 7, and 11 for these additional reasons.

Independent claim 16 is directed to a "system for implementing Incremental Redundancy (IR) operations in a wireless receiver." The elements of claim 16 include: (a) a baseband processor that is operable to receive analog signals corresponding to a data

block and to produce samples of the analog signals; (b) an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block; and (c) a system processor that is operable to receive the soft decision bits of the data block. These elements and their recited functions are fairly taught by Pukkila. The other elements of claim 16 are not fairly taught by Pukkila.

Claim 16 further requires: (d) a plurality of IR processing module registers communicatively coupled to the system processor; and (e) an IR processing module communicatively coupled to the system processor and to the plurality of IR processing module registers; (f) wherein the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver; and (g) wherein the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block. The Office Action cites equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila as teaching each of these elements (d)-(g). For the reasons provided above with respect to claim 1, Pukkila fails to disclose, suggest, or teach these elements (d)-(g). For these reasons, Pukkila fails to anticipate claim 16.

Claims 18-20, 22, 26, and 29 depend from claim 16. Pukkila fails to anticipate these claims for at least the reasons described with respect to claim 16. Claims 18-20, 22, 26, and 29 require additional operations by/with the IR processing module and/or the plurality of IR processing module registers. Pukkila fails to disclose the IR processing module and the plurality of processing module registers. Thus, Pukkila fails to anticipate claims 18-20, 22, 26, and 29 for these additional reasons.

2. Claims 1-7, 9-11, 13-22, 24-26, and 28-31 are not anticipated under 35 U.S.C. 102(e) by Parolari (US 20040081248 A1).

Generally, Parolari is directed to link adaptation in a cellular system, which includes the use of IR processing. In making its anticipation rejection based upon Parolari, the Office Action cites FIG. 5 of Parolari and related text, such cited portions of FIG. 5 reproduced immediately below.

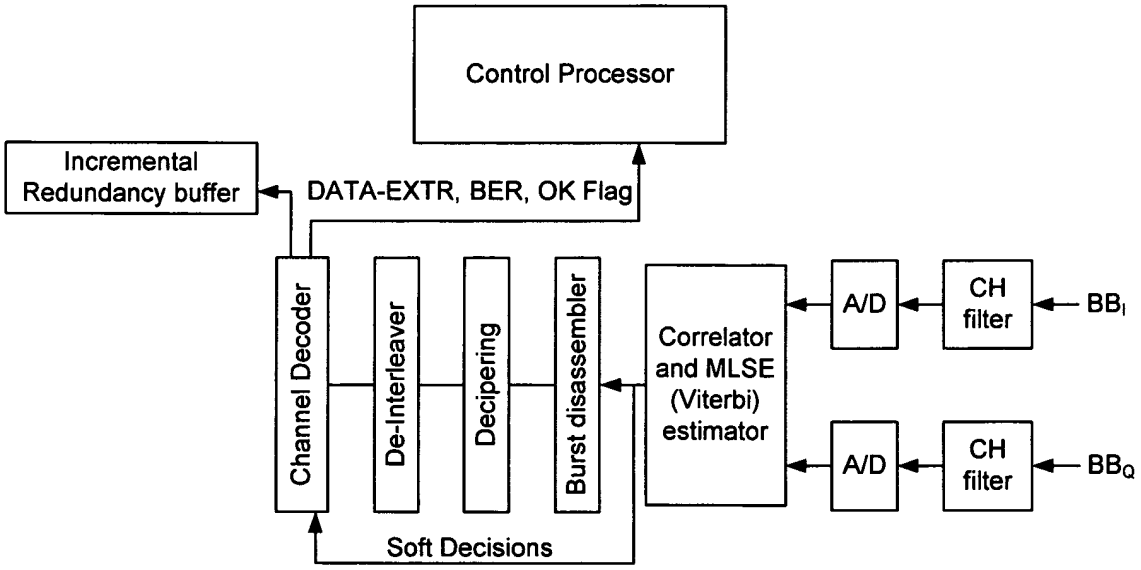

Fig. 5
(Portions of Cited Reference Parolari)

The portions of FIG. 5 reproduced above relate generally to receive processing operations (as do the operations of the pending claims in the present application). Both in-phase (I) and quadrature (Q) signals are received by the Correlator and MLSE (Viterbi estimator). The output of the Correlator and MLSE (Viterbi estimator) are burst disassembled, deciphered, de-interleaved, and channel decoded by corresponding blocks.

A control processor receives input from the channel decoder. An IR buffer receives the output of channel decoder.

Applicants concede that Parolari fairly discloses the elements of (a) receiving, (b) sampling, and (c) equalizing of claim 1. Applicants urge that Parolari fails to disclose, suggest, or teach the elements of (d) configuring, (e) initiating, (f) accessing, or (g) performing of claim 1.

In asserting that Parolari meets all elements (d)-(g) of claim 1, the Office Action cites the block control processor of FIG. 5 described at paragraph [0112] of Parolari as disclosing elements (d), (e), (f), and (g) of claim 1. The Office Action also cites the block channel decoder of FIG. 5 in meeting element (g) of claim 1. Parolari describes at paragraph [0112] (page 11 bottom portion of column):

> "Incremental redundancy strategy supported by an Incremental Redundancy buffer for temporarily storing RLC blocks to be *retransmitted* under ARQ. A buffer overflow activates a signal IRout directed to the Control Processor. Decoded RLC signaling blocks, indicated with DATA-EXTR, are extracted and sent to the Control Processor for the correct interpretation and execution (such as: Power control, Timing Advance, Handover, etc.).

At best, Parolari describes generally how a control processor oversees/controls IR processing and how RLC blocks may be stored in an IR buffer for **retransmission, not storage of received punctured data blocks**. Parolari further describes in its later portions IR processes that may be implemented for link adaptation purposes. However, these details do not disclose any other structure that performs IR processing of received punctured data.

Stated simply, Parolari fails to disclose either an IR processing module or IR processing module registers as illustrated in FIG. 5B of the present application..

The Office Action equates FIG. 5 block control processor paragraph [0112] of Parolari with (d) "configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers" of claim 1. As described above, these portions of Parolari described generally some aspects of an IR process. These and other portions of Parolari do not disclose, suggest, or teach (d) "configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers" as required by claim 1.

The Office Action equates FIG. 5 block control processor paragraph [0112] of Parolari with (e) "initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver" of claim 1. As described above, these portions of Parolari described generally some aspects of an IR process. These and other portions of Parolari do not disclose, suggest, or teach (e) "initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver" as required by claim 1.

The Office Action equates FIG. 5 block control processor paragraph [0112] of Parolari with (f) "accessing, by the IR processing module, the plurality of IR processing module registers" of claim 1. As described above, these portions of Parolari described generally some aspects of an IR process. These and other portions of Parolari do not disclose, suggest, or teach (f) "accessing, by the IR processing module, the plurality of IR processing module registers" as required by claim 1.

The Office Action equates FIG. 5 block channel decoder and control processor paragraph [0112] of Parolari with (g) "performing, by the IR processing module, IR

operations on the soft decision bits of the data block in an attempt to correctly decode the data block." As described above, these portions of Parolari described generally some aspects of an IR process. These and other portions of Parolari do not disclose, suggest, or teach (g) "performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block" of claim 1.

Parolari fails to anticipate claim 1 for any and all of the reasons provided above. Because claims 3-5, 7, and 11 depend from claim 1, Parolari fails to anticipate claims 3-5, 7, and 11 for these same reasons. Claims 3-5, 7, and 11 require additional operations by/with the IR processing module and/or the plurality of IR processing module registers. Parolari fails to disclose the IR processing module and the plurality of processing module registers. Thus, Parolari fails to anticipate claims 3-5, 7, and 11 for these additional reasons.

Independent claim 16 is directed to a "system for implementing Incremental Redundancy (IR) operations in a wireless receiver." The elements of claim 16 include: (a) a baseband processor that is operable to receive analog signals corresponding to a data block and to produce samples of the analog signals; (b) an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block; and (c) a system processor that is operable to receive the soft decision bits of the data block. These elements and their recited functions are fairly taught by Parolari. The other elements of claim 16 are not fairly taught by Parolari.

Claim 16 further requires: (d) a plurality of IR processing module registers communicatively coupled to the system processor; and (e) an IR processing module communicatively coupled to the system processor and to the plurality of IR processing

module registers; (f) wherein the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver; and (g) wherein the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

The Office Action cites the block control processor of FIG. 5 described at paragraph [0112] of Parolari as disclosing elements (d), (e), (f), and (g) of claim 16. The Office Action also cites the block channel decoder of FIG. 5 in meeting element (g) of claim 16. However, Parolari fails to disclose either an IR processing module or IR processing module registers, which are required by elements (d)-(g) of claim 16. For these reasons, Parolari fails to anticipate claim 16.

Claims 18-20, 22, 26, and 29 depend from claim 16. Parolari fails to anticipate these claims for at least the reasons described above with respect to claim 16. Claims 18-20, 22, 26, and 29 require additional operations by/with the IR processing module and/or the plurality of IR processing module registers. Parolari fails to disclose the IR processing module and the plurality of processing module registers. Thus, Parolari fails to anticipate claims 18-20, 22, 26, and 29 for these additional reasons.

3. Claims 8, 12, 23, and 27 are not unpatentable under 35 U.S.C. 103(a) over Parolari in view of Ramesh (U.S. Patent No. 6,909,758 B2).

For the reasons provided above with reference to claims 1 and 16, Parolari fails to meet all of the elements of claims 1 and 16. Ramesh is cited for its teachings relating to depuncturing of punctured data blocks stored in memory. Ramesh fails to meet the shortcomings of Parolari. For these reasons, the combination of Parolari and Ramesh does not meet the limitations of claims 1 and 16. Claims 8 and 12 and claims 23 and 27 depend from claims 1 and 16, respectively. Thus, for the reasons provided above with respect to claims 1 and 16, the combination of Parolari and Ramesh fails to render obvious claims 8, 12, 23, and 27.

G. Conclusions

For the above-provided reasons, the Appellants respectfully request that all of the rejections of the Final Office Action be overturned and that the claims in the present application be allowed to issue.

RESPECTFULLY SUBMITTED,

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CERTIFICATE OF MAILING
37 C.F.R 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:

August 16, 2006 — Date

/Bruce E. Garlick, 36,520/ — Signature

H. Claims Appendix

1. (original) A method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising:

receiving an analog signal corresponding to a data block;

sampling the analog signal to produce samples;

equalizing the samples to produce soft decision bits of the data block;

configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers;

initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver; and

accessing, by the IR processing module, the plurality of IR processing module registers; and

performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

2. (original) The method of claim 1, wherein the data block comprises a complete link layer data block.

3. (original) The method of claim 1, wherein configuring the plurality of IR processing module registers comprises the system processor writing the soft decision bits of the data block to the plurality of IR processing module registers.

4. (original) The method of claim 1, further comprising the system processor

writing the soft decision bits of the data block to a memory accessible by the IR processing module.

5. (original) The method of claim 1, wherein performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block further comprises the IR processing module:

determining that an additional copy of the data block is stored in memory;

retrieving soft decision bits of the additional copy of the data block;

soft combining the soft decision bits of the additional copy of the data block with the soft decision bits of the data block to produce combined soft decision bits of the data block; and

decoding the combined soft decision bits of the data block.

6. (original) The method of claim 5, wherein:

determining that an additional copy of the data block is stored in memory is based upon type I IR memory contents; and

retrieving soft decision bits of the additional copy of the data block includes accessing type II IR memory.

7. (original) The method of claim 5, further comprises the IR processing module identifying an IR mode of the additional copy of the data block stored in memory.

8. (previously presented) The method of claim 7, further comprising, the IR

processing module:

identifying a puncturing pattern of the additional copy of the data block stored in memory; and

depuncturing the copy of the data block stored in memory, when required.

9. (original) The method of claim 5, further comprising assigning different weights to each of the data block and the additional copy of the data block for soft combining.

10. (original) The method of claim 9, wherein weights are assigned to the data block and to the additional copy of the data block based upon respective measured signal qualities.

11. (original) The method of claim 5, further comprising the IR processing module storing the combined soft decision bits of the data block in memory for later use.

12. (original) The method of claim 1, wherein the IR operations performed by the IR processing module include:

decoding the soft decision bits of the data block to produce a decoded header; and

identifying a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header;

depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and

decoding the depunctured soft decision bits.

13. (original) The method of claim 1, further comprising storing the soft decision bits of the data block in IR memory.

14. (original) The method of claim 1, further comprising the IR processing module:

failing to correctly decode a header of the data block; and

discarding the soft decision bits of the data block.

15. (original) The method of claim 1, wherein:

each symbol of the data block is represented by four punctured soft decision bits; and

each symbol of the data block is also represented by five depunctured soft decision bits.

16. (original) A system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising:

a baseband processor that is operable to receive analog signals corresponding to a data block and to produce samples of the analog signals;

an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block;

a system processor that is operable to receive the soft decision bits of the data block;

a plurality of IR processing module registers communicatively coupled to the system processor;

an IR processing module communicatively coupled to the system processor and to the plurality of IR processing module registers;

wherein the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver; and

wherein the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

17. (original) The system of claim 16, wherein the data block comprises a complete link layer data block.

18. (original) The system of claim 16, wherein in configuring the plurality of IR processing module registers, the system processor writes the soft decision bits of the data block to the plurality of IR processing module registers.

19. (original) The system of claim 16, wherein the system processor is further operable to write the soft decisions of the data block to a memory accessible by the IR processing module.

20. (original) The system of claim 16, wherein in performing IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block, the IR processing module is operable to:

determine that an additional copy of the data block is stored in memory;

retrieve soft decision bits of the additional copy of the data block;

soft combine the soft decision bits of the additional copy of the data block with the soft decision bits of the data block to produce combined soft decision bits of the data block; and

decode the combined soft decision bits of the data block.

21. (original) The system of claim 20, wherein the IR processing module is further operable to:

determine that an additional copy of the data block is stored in memory based upon type I IR memory contents; and

retrieve soft decision bits of the additional copy of the data block by accessing type II IR memory.

22. (original) The system of claim 20, wherein the IR processing module is further operable to identify an IR mode of the additional copy of the data block stored in memory.

23. (previously presented) The system of claim 22, wherein the IR processing module is further operable to:

identify a puncturing pattern of the additional copy of the data block stored in memory; and

depuncture the copy of the data block stored in memory, when required.

24. (original) The system of claim 20, wherein different weights are assigned to each of the data block and the additional copy of the data block for soft combining.

25. (original) The system of claim 24, wherein weights are assigned to the data block and to the additional copy of the data block based upon respective measured signal qualities.

26. (original) The system of claim 20, wherein the IR processing module is further operable to store the combined soft decision bits of the data block in memory for later use.

27. (original) The system of claim 16, wherein the IR processing module is further operable to:

decode the soft decision bits of the data block to produce a decoded header; and

identify a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header;

depuncture the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and

decode the depunctured soft decision bits.

28. (original) The system of claim 16, wherein the IR processing module is further operable to store the soft decision bits of the data block in an IR memory.

29. (original) The system of claim 16, wherein the system processor is further operable to store the soft decision bits of the data block in an IR memory.

30. (original) The system of claim 16, wherein the IR processing module is further operable to:

fail to correctly decode a header of the data block; and

discard the soft decision bits of the data block.

31. (original) The system of claim 16, wherein:

each symbol of the data block is represented by four punctured soft decision bits; and

each symbol of the data block is also represented by five depunctured soft decision bits.

I. Evidence Appendix

No Evidence Submitted.

J. Related Proceedings Appendix

No Related Proceedings